TRW

Monthly Report for

12-Bit High Dynamic Range ADC

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1.0 Technical Progress

During this reporting period, detailed preliminary analysis of the maximum ADC sample rate was completed. The results were discussed during a teleconference held on September 4, 1997 (attendees were: G. Nichols, B. Oyama, S. Nelson, M. Englekirk, and B. Wong). Summaries of the analysis results are shown in Figures 1-1 and 1-2. The primary result of the analysis is a change in three design goals for the 12-bit ADC: (1) increased sample rate (213 Msps); (2) increased input frequency range (130 Mhz to 190 Mhz); (3) relaxed SNR/SFDR for near-full scale inputs (50 dB at Pclip). These changes are reflected in Figure 1-3. In addition, a preliminary chip specification (shown in Figure 1-4) was generated to communicate the detailed ADC requirements versus capabilites.

The following is a summary of additional technical notes recorded during the 9/4/97 telecon:

1. ADC Calibration may cause occasional (i.e., infrequent), temporary disruption of the output data; this is acceptable to the system assuming the duration of the disruption is less than 1 msec.
2. There may be a favorable system noise tradeoff if the RF box (which precedes the ADC) can supply a full scale signal power of +4 to +8 dBm; this would allow the ADC to eliminate its internal wideband amplifier (WBA) -- resulting in lower ADC noise and reduced dc power. G. Nichols will investigate the RF output power capability.
3. The ADC spec will be changed to reflect an increased input frequency range of 130 MHz to 190 MHz (60 MHz bandwidth).
4. Overload voltage and recovery time requirements were discussed. G. Nichols will investigate the max RF output under fault conditions; the level of overload will determine whether external clamp diodes are required to protect the ADC IC from damage.
5. Based on the new specification, the ADC will provide 42 dB of dynamic range when maintaining a minimum SNR of ≥20 dB.
6. Gain flatness: we will adapt a 1 dBpp requirement and a 0.5 dBpp goal over the input frequency band of interest.
7. TRW will provide a recommendation for a manufacturer that can provide the required low jitter ADC master clock (aprox. 1500 to 2000 MHz range).
8. TRW will add an over/under-range flag output bit (as a design goal).
9. The baseline digital output interface will be LVDS-compatible. TRW will FAX selected portions of the IEEE 1596.3 spec for LVDS to G. Nichols.
10. G. NIchols will confirm the LVDS I/O capability of the companion CMOS processor ASIC.

12 BIT ADC SIMULATION SUMMARY
(75 Degrees Celsius)

Input Power dBm	Sample Rate Msps	DAC/Resamp Parasitics (ff)	Cell /Folder Parasitics (ff)	Theoretical SNR	SNR dB
0	142.8	0/0	0	74	72.4
0	285.7	0/0	0	74	71.9
0	285.7	100/100	0	74	70.3
0	285.7	200/100	0	74	71.6
0	285.7	100/100	50/20	74	68.8
0	285.7	100/100	50/5	74	70.3
-12	285.7	100/100	50/20	62	63.0
-24	285.7	100/100	50/20	50	52.1
-36	285.7	100/100	50/20	38	37.7

Notes:

1. Input is sampled sine wave - F=19/21 times sample rate
2. 0dB is full scale (2V pp)
3. No WBA or S/H - Resamp is driven from voltage source
4. Parasitics on DAC and Resamp are capacitors tied to outputs.
5. Parasitics on Cell/Folder are capacitors tied to outputs and inputs of most cells and same on inputs to folder
6. Results come from a 21 point DFT with the signal bin nulled and replaced with average bin power for noise calculation.

Conclusions:

1. Dynamic level errors caused by operating the ADC near the speed limit imposed by settling time constraints do not immediately lead to large level errors
2. Dynamic errors tend to disappear as the input signal level drops.

Figure 1-1. Simulation Results for ADC Maximum Speed.

NRL ADC Noise Budget
(Fs = 213 Msps)

Noise Source	dB below full scale	Comment
Level Errors		
0 dBm input, Static	-65	Loading = Pclip
0 dBm input, Dynamic	-65	Loading = Pclip
-12 dBm input, Static	-65	53 dBc, Loading = Pclip-12 dB
-12 dBm input, Dynamic	-	Loading = Pclip-12 dB
Thermal Noise		
400 MHz NBW	-65	High Power WBA
Distortion		
0 dBm input	-60	60 dB SFDR
-12 dBm input	-74	62 dB SFDR
Total		
0 dBm input	-57	57 dB SNR
-12 dBm input	-62	50 dB SNR

Notes:
1. Worst case noise sources

Conclusions

- 7X or 8X master clock enables optimized internal timing allocation to maximize ADC speed
- High speed sacrifices S/H acquisition time and generates some dynamic level errors (near full scale)
- 213 Msps achievable with relaxed SNR requirements for inputs near Pclip.
- ADC can be clocked slower to achieve >70 dB SFDR and >10 effective bits

Figure 1-2. ADC Error Budget and Analysis Conclusions

Parameter	Goal
Resolution	12 bits
Sample Rate	213 Msps
Analog Input Frequency Range	130 MHz to 190 MHz (BW=60 MHz)
SNR, Pclip - 0.5dB	57 dB
Pclip - 12dB	50 dB
Pclip - >12dB	SNR rolls off at 1dB/dB rate
SFDR, Pclip - 0.5dB	60 dB
Pclip - 12 dB	62 dB
ADC Full Scale Input Power	0 dBm (= Pclip)
Output Data Coding	Offset Binary
Input Clock Interface	ac-coupled sinewave (0 +/- 2 dBm)
Output Clock, Data Interface	LVDS-compatible (diff. CMOS)
Power Supply Voltages	+5.5V, -7.5V
Power Dissipation	< 6 watts

Figure 1-3. Revised ADC Performance Goals.

Figure 1-4. 12-Bit ADC Requirements versus Capabilities.

Parameter	Requirement	Capability	Units	Comment
General				
Sample Rate	213	250	Msps	
Resolution	12	12	Bits	
Coding	Offset Binary	Offset Binary	Offset Binary	
Clock	1491	1750	MHz	7X (TBD)
Calibration				Factory Cal
Cal Update Duration	1.0	0.1	msec	Performance is degraded temporarily when cal logic senses temp change
Analog Input				
Clip Level		0	dBm	(= Pclip)
Gain		154	µV/Q	Input referred Q-step
Initial Gain Tolerance		TBD	dB	
Gain Variation		TBD	dB	
Signal Frequency				
min	130	5	MHz	BW=60 MHz IFc=160 MHz
max	190	250	MHz	
Input Offset		20	+/- LSBs	
Input Resistance		50	Ohms	Internal Termination
Input Capacitance		<5	pF	
Overload Voltage	TBD	TBD	dBm	
Recovery Time	100	20	nsec	
AC Performance				
SNR				
P clip - 0.5dB	50	57	dB	
P clip - 12dB	50	50	dB	SNR rolls off classically at 1dB/dB of input power
SFDR				
P clip - 0.5dB	50	60	dB	
P clip - 12dB	50	62	dB	
Gain Flatness	1.0	0.5	dB pp	fin=130 to 190 MHz
Inputs				
Conversion Clock	Single Ended sine wave	Single End sine wave		AC-coupled
Frequency	1491	1750	MHz	7X (TBD)
Duty cycle				
min		40	%	
max		60	%	

Figure 1-4, continued.

Parameter	Requirement	Capability	Units	Comment
Conversion Clock (cont'd.)				
Input Power		0 +/- 2	dBm	
Termination		50	Ohm	
Data				
Data Interface	LVDS -compatible	LVDS -compatible		(Diff. CMOS)
Data Rate	213	250	Msps	
Output Clock	same	same		
Overrange Bit	same	same		Electrically identical to data and clock. Indicates input has exceeded range
Data to Clock skew				
min	TBD	-100	psec	Variation in clock-to-data delay
max	TBD	100	psec	
V swing				
min	250	250	mV	Into 100 Ohm load
max	400	400	mV	
V common mode				
min	0	1000	mV	Nominal Vcm = 1.2V
max	2400	1400	mV	
Power				
Vee		-7.5	V	
Iee		520	mA	(TBD)
Vcc		5.5	V	
Icc		200	mA	(TBD)
Supply Tolerance		+/- 5	%	
Power	6	5	W	
Max Ripple		5	mVrms	
Temperature (ambient)				Performance Range
min	0	-15	C	
max	+70	+85	C	

2. Plans for Next Reporting Period

During the next reporting period, detailed electrical design of the ADC chip will continue. In addition, conceptual design of the ADC subsytem will also continue.

3. Financial Status

The attached table shows the forecasted versus actual expenditures for the Phase 1 program. At month-end August, 1997 we are showing an underrun of $17.8K.

Table 1. Program Expenditures Forecast

Month	Monthly Total ($K)	Cumulative Total ($K)	Cumulative Actuals ($K)	Delta (Forecast - Actuals)
Jun-97	5.3	5.3	2.3	3.0
Jul-97	35.7	41.0	26.4	14.6
Aug-97	42.4	83.4	65.6	17.8
Sep-97	40.7	124.1		
Oct-97	81.1	205.2		
Nov-97	58.4	263.6		
Dec-97	55.2	318.8		
Jan-98	89.1	407.9		
Feb-98	73.0	480.9		
Mar-98	75.7	556.6		
Apr-98	121.8	678.4		
May-98	64.6	743.0		
Jun-98	73.7	816.7		
Jul-98	103.4	920.1		
Aug-98	77.8	997.9		
Sep-98	64.9	1062.8		
Oct-98	72.2	1135.0		
Nov-98	54.0	1189.0		